120

AF/2811

TRANSMITTAL OF APPEAL BRIEF

Docket No.
SON-2010

In re Application of: Hisao Hayashi et al

Application No.	Filing Date	Examiner	Group Art Unit
09/772,986	January 31, 2001	Thien F. Tran	2811

Invention: THIN FILM SEMICONDUCTOR DEVICE, DISPLAY DEVICE USING SUCH THIN FILM SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed: November 25, 2003 .

The fee for filing this Appeal Brief is 330.00 .

[X] Large Entity [ ] Small Entity

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Dated: December 31, 2003

Ronald P. Kananen
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PTO/SB/17 (08-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003, Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	09/772,986
Filing Date	January 31, 2001
First Named Inventor	Hisao Hayashi
Examiner Name	Thien F. Tran
Art Unit	2811
Attorney Docket No.	SON-2010

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

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Deposit Account Number: 18-0013

Deposit Account Name: Rader, Fishman & Grauer PLLC

The Director is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims	4	-** =		x		=	
Independent Claims	1	-** =		x		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	330.00
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 330.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	Ronald P. Kananen	*Registration No. (Attorney/Agent)*	24,104	*Telephone*	(202) 955-3750
Signature				*Date*	December 31, 2003

DC143051.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Hisao HAYASHI et al.	)	Group Art Unit: 2811
	)	
Appln. No.: 09/772,986	)	Examiner: Tran, Thien F.
	)	
Filed: January 31, 2001	)	Conf. No. 2637
	)	
For: THIN FILM SEMICONDUCTOR DEVICE, DISPLAY DEVICE USING SUCH THIN FILM SEMI-CONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	)	

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Alexandria, VA 22313-1450

BRIEF ON APPEAL

Honorable Sir:

This Appeal is taken from the Examiner's Final Rejection dated July 25, 2003 (hereinafter the "Final Office Action") of claims 1-8 and 13-16 in the above-identified application. The Notice of Appeal was filed on November 25, 2003. Submitted herewith are two additional copies of this Appeal Brief. Applicants (hereinafter "Appellants"), respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the present patent application referenced above.

I. REAL PARTY IN INTEREST

The Real "Party-In-Interest" of the present application is Sony Corporation of Tokyo, Japan ("Sony") located at 7-35 Kitashinagawa 6-Chome, Shinagawa-Ku, Tokyo, Japan. An assignment of all rights in the present application to Sony was recorded with the U.S. Patent and Trademark Office on January 31, 2001 at **Reel 011519, Frame 0913**.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-8 and 13-16 are pending, which are the subject of this Appeal. No claims have been allowed.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection. A copy of all claims on appeal is attached hereto as an Appendix.

V. SUMMARY OF THE INVENTION

By way of background, the present invention relates to a thin film semiconductor device for use as a display. Page 1, lines 6-7. The thin film semiconductor device is formed as an integrated circuit on an insulating substrate with bottom gate structured thin film transistors. Page 6, lines 6-10. The gate electrodes of the semiconductor device are positioned at the bottom-most portion of the structure, with the gate insulating film disposed thereover. Page 6, lines 10-12. A semiconductor thin film is then stacked on top of the gate insulating film. The gate electrode is comprised of a metallic material that has a thickness of less than 100nm. Page 6, lines 12-15. Referring to the specification at page 7, lines 24-31, making the thickness of the gate electrode less than 100 nm reduces the thermal capacity of the gate electrode. Additionally, the gate insulating film covering the gate electrodes is comprised of a film, whose thickness is greater than the thickness of the gate electrodes. Page 9, lines 28-30. Making the thickness of the gate electrode less than 100nm reduces the thermal capacity of the gate electrode, which results in a similar thermal condition between the gate electrode and insulating substrate. Page 9, line 31-page 10, line 3. This enlarges the process margin resulting from the laser anneal treatment used during the manufacturing process. Page 10, lines 3-5. Making the thickness of the gate insulating film greater than the thickness of the gate electrode ensures that the benefits of reducing the thickness of the gate electrode below 100 nm are not offset. Page 9, line 28-page 10, line 14. However, if the thickness of the gate insulating film located between the gate electrodes in a semiconductor thin film is too thin, the effect of reducing the thickness of the gate electrode is offset. Page 10, lines 5-7. Accordingly, the thickness of the gate insulating film is designed greater than the thickness of the gate electrodes. Page 10, lines 7-9.

VI. ISSUES PRESENTED

In light of the Final Office Action dated July 25, 2003 (Paper No. 16), the issues presented on this Appeal are whether Claims 1-8 and 13-16 are patentable under 35 USC §103 over Hisao et al (JP 10209467).

VII. GROUPING OF CLAIMS

Claims 1-8, 13-16 stand or fall together.

VIII. ARGUMENTS

The Examiner rejects Claims 1-8 and 13-16 under 35 USC §103 as being unpatentable over Hisao et al (JP 10209467). The Examiner states that the thickness of the gate insulating film *can* be chosen to be thicker than the thickness of the gate electrode. (See office action dated February 7, 2003 at pages 2-3). The Examiner states that the cited reference discloses a gate electrode that is about 100nm thick and a gate insulating film that has a thickness in a range of 100-200 nm. The Examiner states that "assuming" that the insulating film is chosen as thicker than 100nm and "assuming" that the gate electrode is chosen as thinner than 100nm, then Appellant's claimed range would overlap with that of the cited reference. The Examiner states that overlapping ranges in the cited reference create a *prima facie* case of obviousness. Appellant traverses the rejection. MPEP 2144.05 states:

> "Applicants can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP Section 716.02 - Section 716.02(g) for a discussion of criticality and unexpected results."

Merely because it is possible for a claim limitation to exist in a cited reference does not necessarily mean that a cited reference actually teaches that claim limitation. This is exactly the case here. The Examiner asserts that it is *possible* for the cited reference to disclose that the gate insulating film is thicker than the gate electrode. The support for this reasoning is the Examiner's assumption that the specific values of the disclosed ranges are chosen in such a way as to overlap with the specific values recited in the claims. However,

what is overlooked is that the cited reference completely fails to present any reasoning whatsoever as to why one would adjust the disclosed relationship between the gate insulating film and the gate electrode in the cited reference to arrive at Appellant's claimed invention. In fact, the reference is completely silent as to any relationship whatsoever between the gate insulating film and gate electrode, as well as any reasoning as to why one would provide any specific relationship between the gate insulating film and the gate electrode.

Alternatively, the specification of the present application discloses specific attributes in making the gate electrode less than 100nm and making the gate insulating film greater in thickness than the gate electrode. Referring to the specification at page 7, lines 24-31, making the thickness of the gate electrode less than 100 nm reduces the thermal capacity of the gate electrode. This enlarges the process margin resulting from the laser anneal treatment used during the manufacturing process. Page 10, lines 3-5. Making the thickness of the gate insulating film greater than the thickness of the gate electrode ensures that the benefits of reducing the thickness of the gate electrode below 100 nm are not offset. Page 9, line 28-page 10, line 14. Accordingly, the thickness of the gate insulating film is claimed as greater than the thickness of the gate electrode. Page 10, lines 7-9. Therefore, to the extent that the Examiner asserts that a *prima facie* case of obviousness is presented by virtue of this alleged overlapping range, such a *prima facie* case is properly rebutted by Appellant's express recitation of the claimed relationship and of the significant advantages obtained therefrom, especially in view of the failure by the cited reference to present any reasoning as to why such a range relationship would exist. Accordingly, for the reasons set forth above, the Examiner's rejection of Claims 1-8 and 13-16 should be reversed.

V. CONCLUSION

Appellant respectfully submits that all of the appealed claims in this application (Claims 1-8, 13-16) are patentable for at least the reasons stated above and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate. It is believed that any fees due with respect to this paper have been identified in any transmittal accompanying this paper. However, if any additional fees are required in connection with the filing of this paper that are not identified in any accompanying transmittal, permission is given to charge account number 18-0013 in the name of Rader, Fishman and Grauer PLLC.

Respectfully submitted,

Dated: Dec. 29, 2003

By: _____

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APPENDIX OF CLAIMS ON APPEAL – CLAIMS 1-8 and 13-16

1. A thin film semiconductor device comprising:

an insulating substrate; and

a thin film transistor formed on said insulating substrate, wherein

said thin film transistor is formed in a bottom gate structure having gate electrode, a gate insulating film, and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100nm;

said gate insulating film has a thickness that is greater than said thickness of said gate electrode.

2. The thin film semiconductor device according to Claim 1, wherein

said gate insulating film has a thickness thicker than the thickness of said gate electrode.

3. The thin film semiconductor device according to Claim 1, wherein

said semiconductor thin film comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

4. The thin film semiconductor device according to Claim 1, wherein

said gate electrode has a multi-layered structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

5. A display device comprising:

an insulating substrate;

pixels arranged in a matrix form; and

thin film transistors for driving said respective pixels, wherein said pixels and said thin film transistors are formed as integrated circuits on said insulating substrate, each of said thin film transistors has a bottom gate structure having a gate electrode, a gate insulating film and a semiconductor thin film stacked in the order from below upward, and

said gate electrode is made of metallic material having a thickness of less than 100 nm;

said gate insulating film has a thickness that is greater than said thickness of said gate electrode.

6. The display device according to Claim 5, wherein

said gate insulating film has a film thickness thicker than the thickness of the gate electrode.

7. The display device according to Claim 5, wherein

said semiconductor thin film comprises polycrystalline silicon crystallized by an irradiation of a laser beam.

8. The display device according to Claim 5, wherein

said gate electrode has a multi-layer structure stacked with an upper layer having comparatively low heat conductivity and high electric resistance, and a lower layer having comparatively high heat conductivity and low electric resistance.

13. The thin film semiconductor device according to Claim 1, wherein the thickness of the gate insulating film is greater than 100 nm.

14. The thin film semiconductor device according to Claim 13, wherein the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.

15. The display device according to Claim 5, wherein the thickness of the gate insulating film is greater than 100 nm.

16. The display device according to Claim 15, wherein the thickness of the gate insulating film is 110 nm and the thickness of the gate electrode is 90 nm.